AMENDMENTS TO THE CLAIMS

Listing of the claims:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

1. (Currently Amended) A power supply noise analysis model generator adapted to model power supply layers in a circuit board and having a processor for processing data of processing sections, said generator comprising:

a CAD data obtaining section that obtains CAD data for the circuit board including information concerning a board shape, pattern shapes, and elements mounted on the circuit board;

a CAD data conversion processing section that converts said CAD data for the circuit board into power supply island pattern data, element data, lead pattern data, and via pattern data;

a power supply pair extraction processing section that extracts two power supply island patterns as a power supply pair when any two power supply islands existing in two different power supply layers, respectively, in any regions across the entire circuit board, overlap each other, the overlap being determined from the CAD data when any two power supply islands overlap each other, in any regions across the entire circuit board, in plan view from a top side of the circuit board and the patterns of all pairs of overlapping power supply islands across the entire circuit board are extracted by the power supply pair extraction processing section;

a node layout processing section that positions plural nodes on a power supply pair region which is occupied by each power supply pair on a plane of said circuit board;

a node region determination processing section that determines node regions surrounding said nodes, respectively;

an impedance parameter determination processing section that determines impedance parameters expressing relationships between said nodes, respectively;

a power supply layer model generation processing section that connects said nodes to each other using said impedance parameters, to generate a power supply layer model; and

a power supply noise analysis model generation processing section that connects said power supply layer model, said lead pattern data and said via pattern data to one another to generate a power supply noise analysis model supplied to a user ~~physically or electronically~~ by said power supply noise analysis model generator.

2. (Original) The power supply noise analysis model generator according to claim 1, wherein said impedance parameters are a reactance L, a resistance R, and an interlayer capacitance C.

3. (Original) The power supply noise analysis model generator according to claim 1, wherein if a power supply pair space sandwiched between power supplies of an observed power supply pair is contacted or overlapped by another power supply pair space of any other power supply pair, said power supply pair extraction processing section makes said observed power supply pair and said other power supply pair into a group.

4. (Original) The power supply noise analysis model generator according to claim 1, further comprising a ripple processing section that positions, on said power supply pair region, ripples which are wave fronts of electromagnetic waves radiated into said power supply pair region from said elements, wherein said node layout processing section positions said nodes, based on pitches of said ripples.

5. (Original) The power supply noise analysis model generator according to claim 4, wherein said ripple processing section uses rising or falling times of those of said elements which are mounted on said power supply pair region, maximum operating frequencies of those elements, and areas of said ripples, to calculate intervals between said ripples.

6. (Original) The power supply noise analysis model generator according to claim 4, wherein said ripple processing section spreads said ripples into power supply pair regions of power supply pairs which belong to a group.

7. (Original) The power supply noise analysis model generator according to claim 4, further comprising a ripple display processing section that searches for outline coordinates of said ripples, and displays said ripples with the use of said outline coordinates.

8. (Currently Amended) The power supply noise analysis model generator according to claim 1, further comprising a mesh division processing section

that divides said power supply pair region with the use of meshes based on a wavelength of one of said elements that is mounted on said power supply pair region of the circuit board that has the highest operating frequency.

9. (Original) The power supply noise analysis model generator according to claim 8, further comprising an internal data storage which stores information for every of said meshes into a table on which coordinates on said circuit board correspond to addresses.

10. (Original) The power supply noise analysis model generator according to claim 9, wherein the information for every of said meshes includes at least one of a ripple level which indicates the number of ripples from an element to a corresponding mesh, the presence or absence of a node in said corresponding mesh, and a node region identifier expressing a node region to which said corresponding mesh belongs.

11. (Original) The power supply noise analysis model generator according to claim 1, wherein, taking a most adjacent node as the node closest to an observed node within a sector having a predetermined radius about said observed node as the center of said sector, said node region determination processing section searches for adjacent nodes by rotating said sector about said observed node.

12. (Original) The power supply noise analysis model generator according to claim 11, wherein said node region determination processing section removes a

square from said power supply pair region thereby to determine an edge of the node region of said observed node with respect to said most adjacent node, said square having as an edge a perpendicular bisector of a predetermined length between said observed node and said most adjacent node and containing said most adjacent node, so that edges of said node region of said observed node are sequentially determined with respect to all the adjacent nodes, respectively, in the order of increasing distance from said most adjacent node, finally to determine the node region of said observed node.

13. (Original) The power supply noise analysis model generator according to claim 1, wherein said impedance parameter determination processing section determines a reactance L and a resistance R based on distances between said nodes, and determines an interlayer capacitance C with the use of the areas of said node regions and a distance or distances between power supply layers, and said power supply layer model generation processing section arranges said reactance L and said resistance R between nodes on an upper surface of each power supply pair and between nodes on a lower surface of each power supply pair, and arranges each interlayer capacitance C between such a couple of nodes that are arranged at equal positions respectively on the upper and lower surfaces of said power supply pair.

14. (Original) The power supply noise analysis model generator according to claim 1, further comprising a power supply noise analysis model storage that stores said power supply noise analysis model.

15. (Original) The power supply noise analysis model generator according to claim 1, wherein said power supply noise analysis model generation processing section further generates a total circuit model in which said power supply noise analysis model is connected to said element data, and stores said total circuit model into said power supply noise analysis model storage.

16. (Currently Amended) A power supply noise analysis model generator which models a power supply layer in a circuit board and having a processor for processing data of processing sections, said generator comprising:

a power supply pair extraction processing section that extracts, as power supply pairs, all of any two different power supply layers located in any regions across the entire circuit board, that overlap each other in a plan view from a top side of the circuit board, said overlap being determined from data indicative of said circuit board; and

a power supply noise analysis model generation processing section that uses said power supply pairs extracted to generate a power supply noise analysis model.

17. (Currently Amended) A power supply noise analysis model generation method of modeling power supply layers in a circuit board, said method comprising:

a step of obtaining CAD data for the circuit board including information concerning a board shape, pattern shapes, and elements;

a step of converting said CAD data for the circuit board into power supply island pattern data, element data, lead pattern data, and via pattern data;

a step of determining, via said CAD data for the circuit board, all power supply island patterns existing in two different layers, respectively, that overlap each other in plan view from a top side of the circuit board;

a step of extracting all power supply island pairs determined to overlap each other, in any regions across the entire circuit board, in plan view from a top side of the circuit board as power supply island pairs;

a step of positioning plural nodes on a power supply pair region which is occupied by each power supply pair on a plane of said circuit board;

a step of determining node regions surrounding said nodes, respectively;

a step of determining impedance parameters expressing relationships between said nodes, respectively;

a step of connecting said nodes to each other using said impedance parameters, to generate a power supply layer model; and

a step of connecting said power supply layer model, said lead pattern data, and said via pattern data to one another to generate a power supply noise analysis model.

18. (Original) The power supply noise analysis model generation method according to claim 17, wherein said impedance parameters are a reactance L, a resistance R, and an interlayer capacitance C.

19. (Original) The power supply noise analysis model generation method according to claim 17, wherein in said step of extracting a power supply pair, if a power supply pair space sandwiched between power supplies of an observed power supply

pair is contacted or overlapped by another power supply pair space of any other power supply pair, said observed power supply pair and said other power supply pair are made into a group.

20. (Original) The power supply noise analysis model generation method according to claim 17, further comprising a step of positioning, on said power supply pair region, ripples which are wave fronts of electromagnetic waves radiated into said power supply pair region from said elements, wherein in said step of positioning plural nodes, said nodes are positioned based on pitches of said ripples.

21. (Original) The power supply noise analysis model generation method according to claim 20, wherein in said step of positioning ripples, rising or falling times of those of said elements which are mounted on said power supply pair region, maximum operating frequencies of those elements, and areas of regions of said ripples are used to calculate said ripples.

22. (Original) The power supply noise analysis model generation method according to claim 20, wherein in said step of positioning ripples, said ripples are spread into power supply pair regions of power supply pairs which belong to a group.

23. (Original) The power supply noise analysis model generation method according to claim 20, further comprising a step of searching for outline coordinates of said ripples, and displaying said ripples with the use of said outline coordinates.

24. (Currently Amended) The power supply noise analysis model generation method according to claim 17, further comprising a step of dividing said power supply pair region with the use of meshes based on a wavelength of one of said elements that is mounted on said power supply pair region of the circuit board that has the highest operating frequency.

25. (Original) The power supply noise analysis model generation method according to claim 24, further comprising a step of storing information for every of said meshes into a table on which coordinates on said circuit board correspond to addresses.

26. (Original) The power supply noise analysis model generation method according to claim 25, wherein said information for every of said meshes includes at least one of a ripple level which indicates the number of ripples from an element to a corresponding mesh, the presence or absence of a node in said corresponding mesh, and a node region identifier expressing a node region to which said corresponding mesh belongs.

27. (Currently Amended) A power supply noise analysis model generation method of modeling a power supply layer in a circuit board, said method comprising:

a step of determining all pairs of power supply island patterns existing in two different layers, respectively, that overlap each other, in any regions across the entire circuit board, in plan view from a top side of the circuit board;

a step of extracting, as power supply pairs, each pair of two different power supply layers that overlap each other, in any regions across the entire circuit board, in a plan view from a top side of the circuit board, said overlap being determined from data indicative of said circuit board; and

a step of generating a power supply noise analysis model by using said power supply pairs thus extracted.

28. (Currently Amended) A computer readable medium encoded with a power supply noise analysis model generation program for modeling power supply layers in a circuit board, said program including executable instructions which when executed by a computer ~~stored in a medium readable by a computer to~~ make said computer execute ~~modeling power supply layers in a circuit board, said program being operable to make the computer execute~~:

a step of obtaining CAD data for the circuit board including information concerning a board shape, pattern shapes, and elements;

a step of converting said CAD data for the circuit board into power supply island pattern data, element data, lead pattern data, and via pattern data;

a step of determining, via said CAD data for the circuit board, all pairs of power supply island patterns existing in two different layers, respectively, of the circuit board,

in any regions across the entire circuit board, that overlap each other in plan view from a top side of the circuit board;

a step of extracting all pairs of power supply islands existing in two different layers, respectively, in any regions across the entire circuit board, that overlap each other as a power supply pairs;

a step of positioning plural nodes on a power supply pair region which is occupied by each power supply pair on a plane of said circuit board;

a step of determining node regions surrounding said nodes, respectively;

a step of determining impedance parameters expressing relationships between said nodes, respectively;

a step of connecting said nodes to each other using said impedance parameters, to generate a power supply layer model; and

a step of connecting said power supply layer model, said lead pattern data, and said via pattern data to one another to generate a power supply noise analysis model.

29. (Currently Amended) The computer readable medium encoded with a power supply noise analysis model generation program according to claim 28, wherein said impedance parameters are a reactance L, a resistance R, and an interlayer capacitance C.

30. (Currently Amended) The computer readable medium encoded with a power supply noise analysis model generation program according to claim 28, wherein in said step of extracting a power supply pair, if a power supply pair space

sandwiched between power supplies of an observed power supply pair is contacted or overlapped by another power supply pair space of any other power supply pair, said observed power supply pair and said other power supply pair are made into a group.

31. (Currently Amended) The computer readable medium encoded with a power supply noise analysis model generation program according to claim 28, further comprising a step of making said computer execute positioning, on said power supply pair region, ripples which are wave fronts of electromagnetic waves radiated into said power supply pair region from said elements, wherein in said step of positioning plural nodes, said nodes are positioned based on pitches of said ripples.

32. (Currently Amended) The computer readable medium encoded with a power supply noise analysis model generation program according to claim 31, wherein in said step of positioning ripples, rising or falling times of those of said elements which are mounted on said power supply pair region, maximum operating frequencies of those elements, and areas of regions of said ripples are used to calculate said ripples.

33. (Currently Amended) The computer readable medium encoded with a power supply noise analysis model generation program according to claim 31, wherein in said step of positioning ripples, said ripples are spread into power supply pair regions of power supply pairs which belong to a group.

34. (Currently Amended) The computer readable medium encoded with a power supply noise analysis model generation program according to claim 31, further comprising a step of making said computer execute searching for outline coordinates of said ripples, and displaying said ripples with the use of said outline coordinates.

35. (Currently Amended) The computer readable medium encoded with a power supply noise analysis model generation program according to claim 28, further comprising a step of making said computer execute dividing said power supply pair region with the use of meshes based on a wavelength of one of said elements that is mounted on said power supply pair region of said circuit board that has the highest operating frequency.

36. (Currently Amended) The computer readable medium encoded with a power supply noise analysis model generation program according to claim 35, further comprising a step of making said computer execute storing information for every of said meshes into a table on which coordinates on said circuit board correspond to addresses.

37. (Currently Amended) The computer readable medium encoded with a power supply noise analysis model generation program according to claim 36, wherein said information for every of said meshes includes at least one of a ripple level which indicates the number of ripples from an element to a corresponding mesh, the

presence or absence of a node in said corresponding mesh, and a node region identifier expressing a node region to which said corresponding mesh belongs.

38. (Currently Amended) A computer readable medium encoded with a power supply noise analysis model generation program for ~~stored in a medium readable by a computer to make said computer execute~~ modeling a power supply layer in a circuit board, said program being operable to make said computer execute:

a step of determining, via data indicative of said circuit board, all pairs of power supply island patterns existing in two different layers, respectively, of the circuit board that overlap each other in plan view from a top side of the circuit board;

a step of extracting all pairs of power supply islands existing in two different layers, respectively, in any regions across the entire circuit board that overlap each other as a power supply pairs;

a step of extracting, as power supply pairs, each pair of two different power supply layers determined to overlap each other in any regions across the entire circuit board; and

a step of using said power supply pairs thus extracted, to generate a power supply noise analysis model.